REMARKS

Claims 1-44 are pending. Claims 1-7, 11, 12, 14-22, 26, and 37-40 including independent claims 1 and 16 were rejected under 35 U.S.C. 102(e) as being anticipated by Dick (6,600,788). Dependent claims 8-10, and 23-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Shung ("An integrated CAD System for Algorithm-Specific IC Design", IEEE Transactions on Computer Aided Design, Vol. 10, No. 4, April 1991). Claims 13, 27-29, and 41-44 including independent claim 41 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Shung and further in view of Saramaki ("Design of Computationally Efficient Interpolated FIR Filters, IEEE Transactions on Circuits and Systems, Vol. 35, No. 1, January 1998).

The Examiner's Conference with Mary C. Hogan is gratefully acknowledged. During the Examiner's Conference, the Applicants discussed the cited art references and claim language. More specifically, the Applicants noted that Dick describes an implementation similar to the materials provided in the background section of the present application. The Applicants believe the claims are patentable in their present form. An amendment to claim 1 has been made to facilitate prosecution. The Examiner noted that although an additional search may be needed, the amendments clarify distinctions between the cited art and the claims.

The Examiner rejected claims 1 and 16 under 35 U.S.C. 102(e) as being anticipated by Dick. Dick notes that "The equations that define the transfer function of predictor filter 40 ... should be implemented in a mathematical modeling environment, such as Matlab, and simulations [are] performed until a predictor length that satisfied the specific problem is determined experimentally." (column 7, lines 23-30) Dick proceeds to noted that "in the present invention, the multipliers (4x12 bit) each consume only 8 CLBS. Therefore, even including the additional resources required to implement modulator 12, the CLB count is 3002. Thus, the present invention consumes only 39% of the logic resources of a prior art direct implementation." (column 7, lines 62-67).

Claims 1 and 16 explicitly recite a filter compiler comprising "a filter resource estimator coupled to the filter spectral response simulator for estimating an implementation cost of the filter." Dick does not teach or suggest a filter compiler including a "filter resource estimator" nor does it teach or suggest a "filter resource estimator coupled to the filter spectral response

simulator." The Examiner argues that Dick describes a filter spectral response simulator (4:8-12). The material cited by the Examiner only notes that the FIR filter "can be configured to provide a variety of transfer functions, including low pass, high pass, and bandpass. As known by those skilled in the art, the desired transfer function is determined by selection of filter coefficients a.sub.0 and a.sub.N-1."

No "resource estimator is coupled to the filter spectral response simulator." The Examiner argues that Dick describes a filter resource estimator. However, the material cited by the Examiner only notes that "In a prior art implementation ... the total cost of a direct implementation of a FIR filter is 7672 CLBs... In contrast, in the present invention, ... the CLB count is 3002. Thus, the present invention consumes only 39% of the logic resources of a prior art direct implementation" (7:51-57). The material cited by the Examiner does not teach or suggest a filter resource estimator and mentions only a resource calculation. Dick makes no mention of having "filter resource estimator" "coupled to the filter spectral response simulator for estimating an implementation cost of the filter" as recited in the claims. Consequently, the rejection to independent claims 1 and 16 is believed overcome.

The Examiner argued that on page 8 of the 12/17/04 office action that "it is understood to one skilled in the art that after the filter is designed using the simulator, the estimate of the resources, or "real estate" the design will take up on the FPGA will be determined and once the design meets the requirements of the specification in terms of performance and resources, the design is then compiled for implemention on the FPGA."

However, neither Dick nor any understanding by one of skilled in the art teaches or suggests a "resource estimator is coupled to the filter spectral response simulator." The Examiner is believed to be referring to a prior art implementation described in the Background section of the present application. More specifically, "Based upon the desired filter response, the behavioral characteristics of the FIR filter are then determined based upon floating-point values that are converted to fixed-point filter coefficients. Once the particular filter coefficients have been calculated, the an interim hardware filter architecture is determined. By hardware filter architecture it is meant whether the FIR filter is to be configured as a parallel or serial type FIR filter. In some applications, a serial type FIR filter configuration may be appropriate whereas in other applications a parallel type FIR filter configuration may be appropriate. A simulation must then be iteratively run on the interim hardware filter architecture to ascertain whether or not FIR

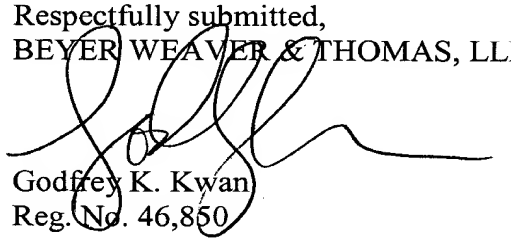
filter, as currently configured, meets the original design specifications. Once an appropriate filter design has been established based upon an acceptable simulation run, the FIR filter design is synthesized and fitted to a target PLD by an appropriate placing and routing program. Typical cycle times for the conventional FIR filter design cycle described above take on the average, at least 6 weeks to complete." (page 3, line 13 – page 4, line 6)

Synthesizing and fitting a design to a target PLD is not a "resource estimator is coupled to the filter spectral response simulator."

Although Applicants believe the claims are allowable in their current form, claim 1 is being amended to facilitate prosecution. Independent claim 1 has been amended to recite "wherein cost analysis is performed substantially in parallel with a performance analysis." Support for this amendment can be found on page 10, lines 19-20. None of the references cited by the Examiner teaches or suggest this element.

In light of the above remarks relating to independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100